PATENT
Attorney Docket No. 61902.000004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of :	)	
	)	
James HAKEWILL, et al.	)	Group Art Unit: 2123
	)	
Serial No.: 09/418,663	)	Examiner: E. Garcia-Otero
	)	
Filed: October 14, 1999	)	
	)	
For: METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN	)	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

DECLARATION OF PETER HUTTON UNDER 37 C.F.R. § 1.132

I, Peter Hutton, a citizen of the United Kingdom, hereby declare and state as follows:

1. I am Vice President of SoC (System on-Chip) products of ARC International ("ARC"), assignee of U.S. Patent Application No. 9/418,663 (the '663 Application from hereon) which describes the claimed ARC proprietary technology (the ARC invention). The ARC invention is included or used in ARC Processor Configuration Tool (ARChitect™), ARChitect2™, ARCtangent™ processors, ARC™ 600 processors, ARC™ 700 processors (including those products listed in Attachment B), SoC (System-On-Chip) products, and Embedded Software products, referred to collectively as "ARC Products".

2. I have over 20 years experience in IP (intellectual property) and IC (integrated circuits) companies. From 1998 to 2002, I worked for Cadence Design Systems Limited, where I held the position of Design Center Manager and was responsible for the largest Cadence IC Design Center. Under my management, the design center generated designs with multiple

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processor cores and was responsible for establishing and running Cadence's soft IP business. Previously in Cadence, from 1997 to 1998, I was Design Centre Manager in Bracknell and, from 1992 to 1996, I was Senior Solution Architect and was involved in consulting and technical sales. From 1982 to 1986, I worked for Unisys where I was a processor designer. Later, I also worked for ES2 and Plessey Research.

3. I have access to and personal knowledge of ARC's confidential sales information, and market share research related to ARC products.

4. I have read the '663 application.

5. I have been asked to submit this declaration to demonstrate the commercial success of ARC's products.

6. ARC licenses and sells microprocessor and integrated embedded system solutions, that include or result from the invention claimed in the '663 application. For example, claim 12, as it is presently amended, covers an integrated circuit, fabricated using the method comprising: creating a customized description language model of an integrated circuit design by receiving one or more inputs from a user for at least one customized parameter of the integrated circuit; receiving an identification of a location of one or more library files that provide at least one prototype description and at least one extension logic description for the integrated circuit for which a model is being generated; and generating through an automated process a customized description language model based on at least one customized parameter, the at least one prototype description, and the at least one extension logic description, the automated process including the acts of reading at least one prototype description and modifying the at least one prototype description by substituting values in the at least one prototype description or merging additional descriptions based on the at least one customized parameter; generating a netlist which

is descriptive of the circuitry of said integrated circuit; compiling said netlist and said hardware description model to produce a compiled integrated circuit design; fabricating at least one mask or FPGA configuration file representing said compiled integrated circuit design; and fabricating said integrated circuit using said at least one mask or FPGA configuration file; wherein said act of creating is performed at a high level of abstraction, thereby allowing developers to customize processor designs for a specific application. Other features and limitations of the invention claimed in the '663 application are also present in the configuration tool for customizing processor design.

7. As a result of my position with ARC, I am familiar with ARC's past and present products and consumer preferences in the microprocessor IP.

8. Until ARC introduced the ARChitect Processor Configuration Tool, there was an unsolved need in the area of processor design. The invention of the '663 application solves this need by providing an automated design tool that enables ASIC (Application Specific Integrated Circuit) developers to choose CPU extensions and configuration options through a GUI (Graphical User Interface). The ARChitect Processor Configuration Tool has been well received by ARC's customers who are taking advantage of the unique capabilities of configurable processors and configurable tools-capabilities that standard parts with fixed architectures cannot match.

9. During the second quarter of 2003, 2.5 million licensed chips incorporating ARC's invention were sold generating royalty revenue of $ 453,141. Licensed sales of chips with ARC's invention increased dramatically over successive quarters, and in the first quarter of 2004, ARC sold 14.7 million licensed chips with royalty revenue of $1,406,896, as this resulted

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in an increase in total chip sales of 495%, and an increase of revenue of 210%. *See* **Attachment A.**

11. Shortly after the introduction of the ARChitect configuration tool, ARC's market share began to increase, and many well known industry leaders began licensing ARC's processors as evidenced by the list of current licensees. *See* **Attachment B.**

12. In October of 1999, ARC began full distribution and licensing of the ARChitect configuration tool product, which is used in designing customized, and configurable processors in accordance with the teachings of the '663 application. A sample sales brochure for the ARChitect Configuration Tool product is attached hereto as **Attachment C.**

13. The customized, and configurable processors designed in accordance with the teachings of the '663 application received numerous industry awards, such as nominations for the 2003 Microprocessor Report Analyst's Choice for the ARC 600 in the 'Soft IP Processor Cores' category, and the 2002 Microprocessor Report Analyst's Choice for the ARCtangent-A5 in the 'Embedded IP Processor' category.

14. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements an the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

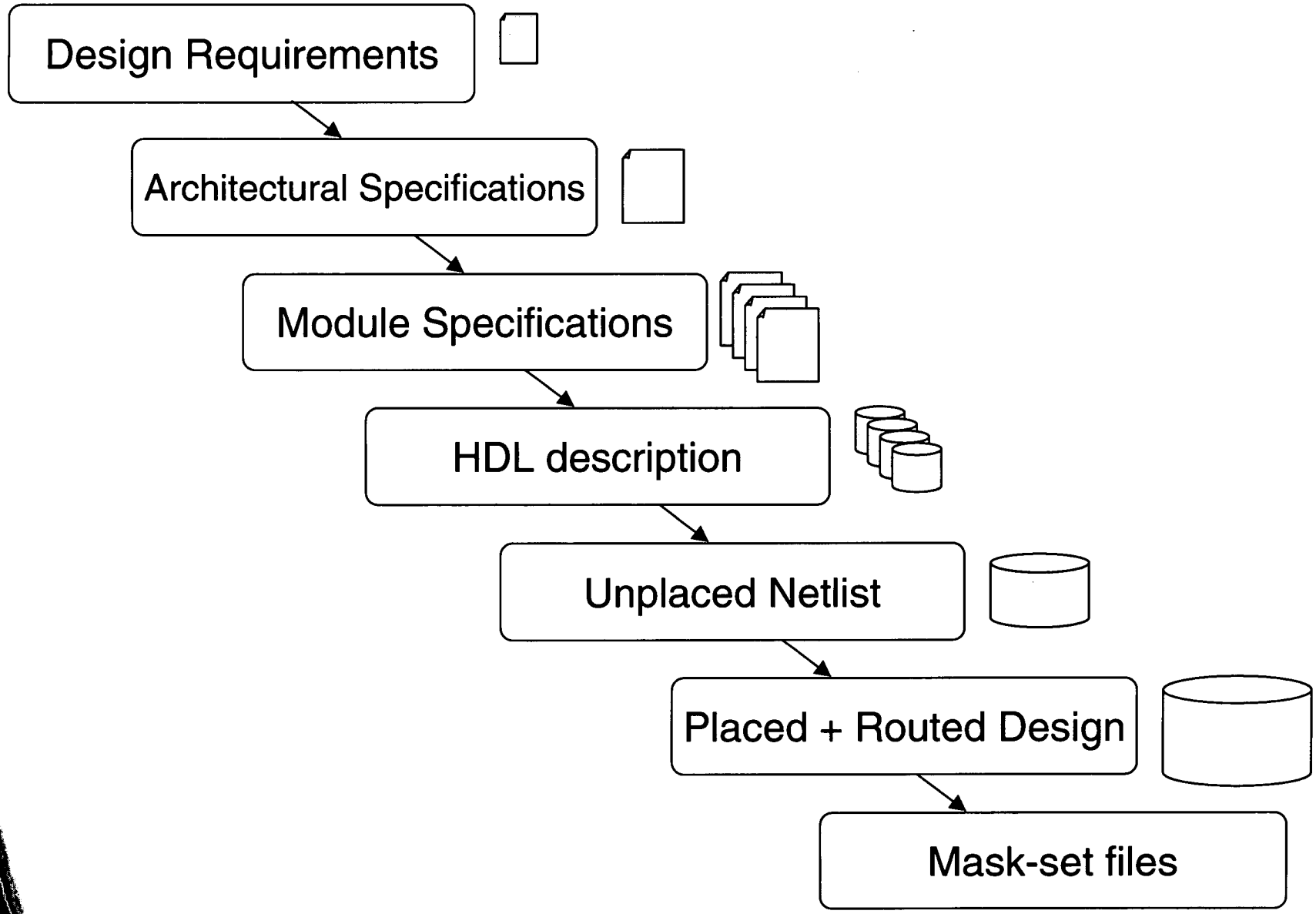
Peter Hutton

Peter Hutton, VP of System on-Chip - ARC International

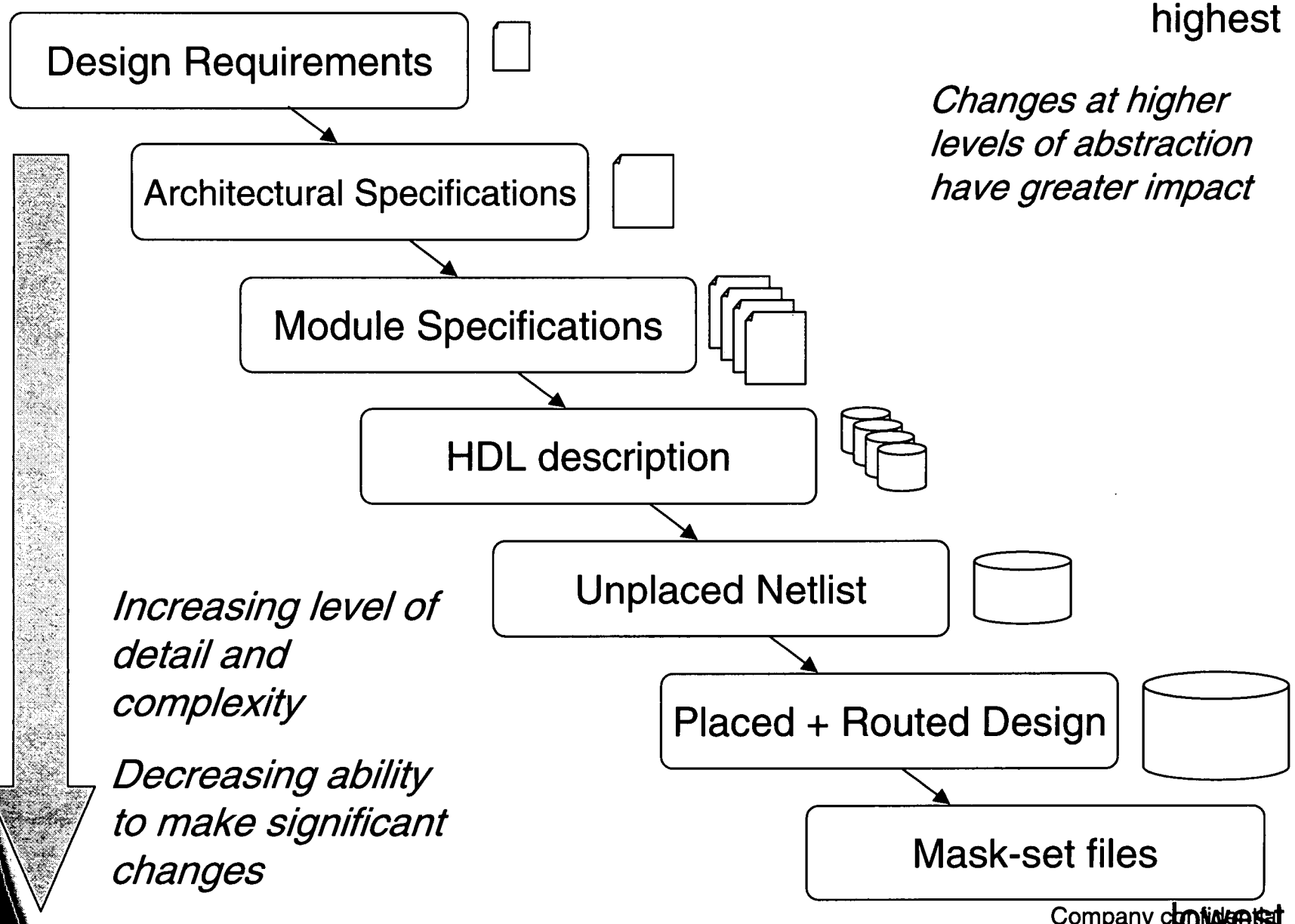
DATE: 28th April 2004

TM

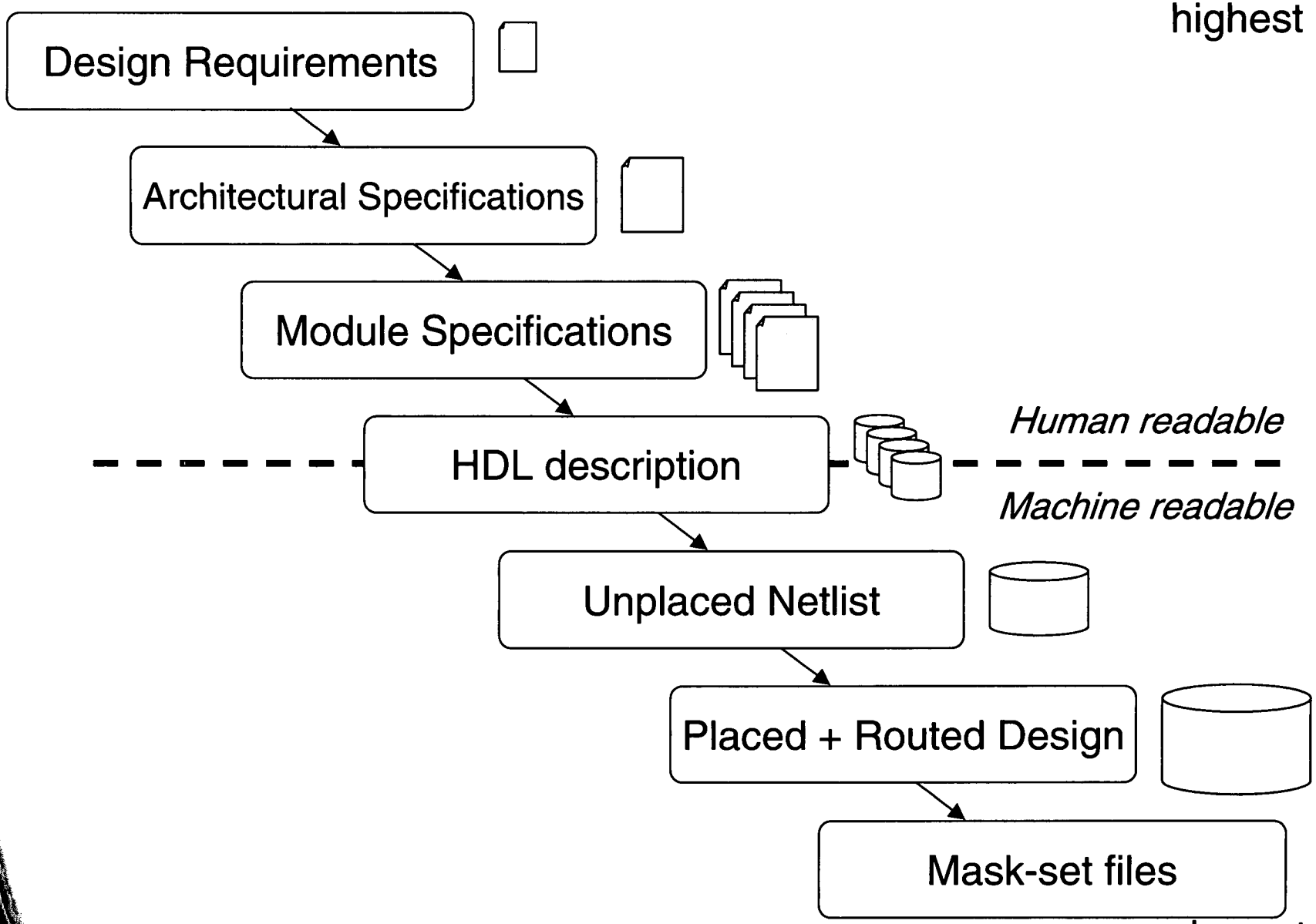
Levels of abstraction



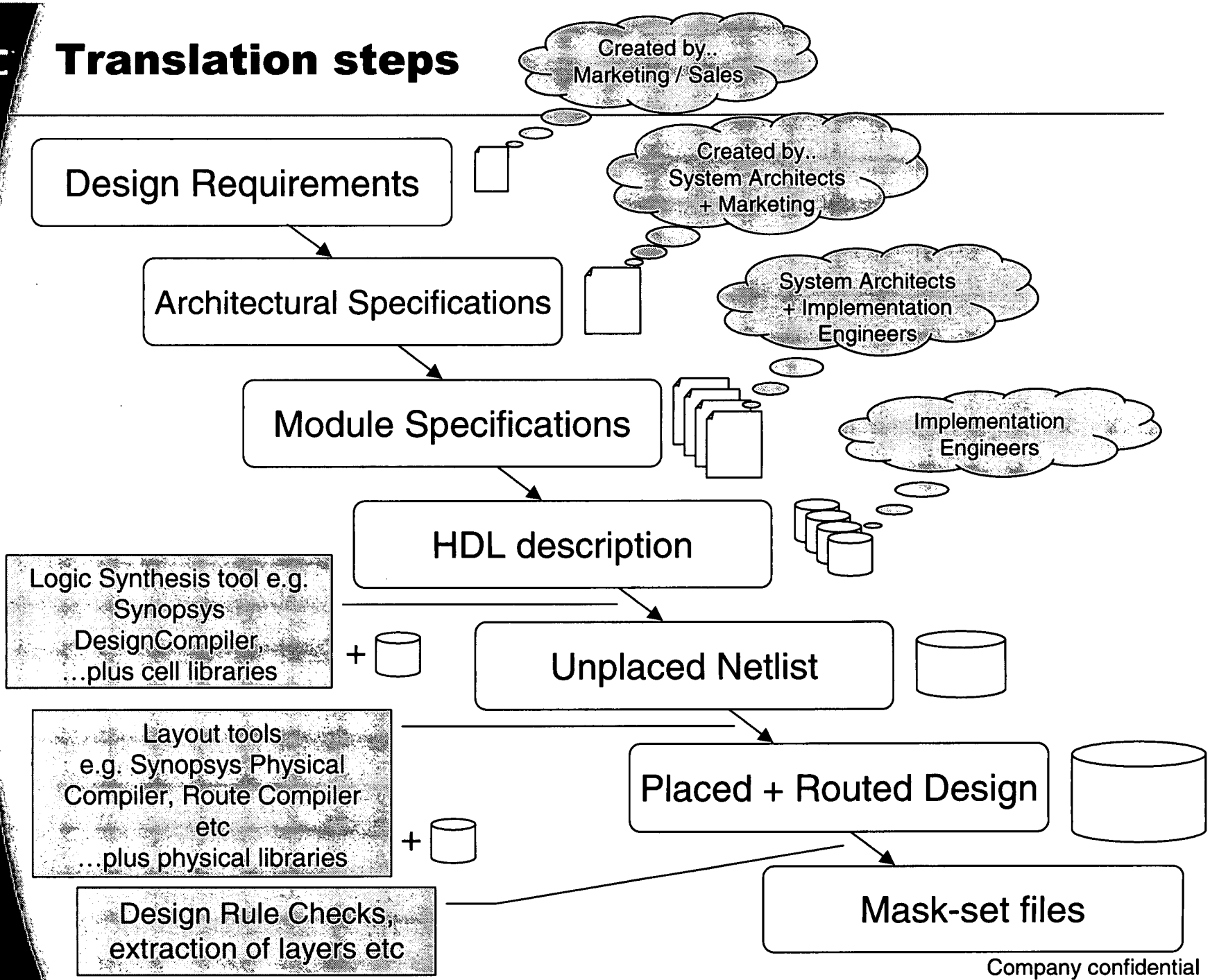
Levels of abstraction



Levels of abstraction



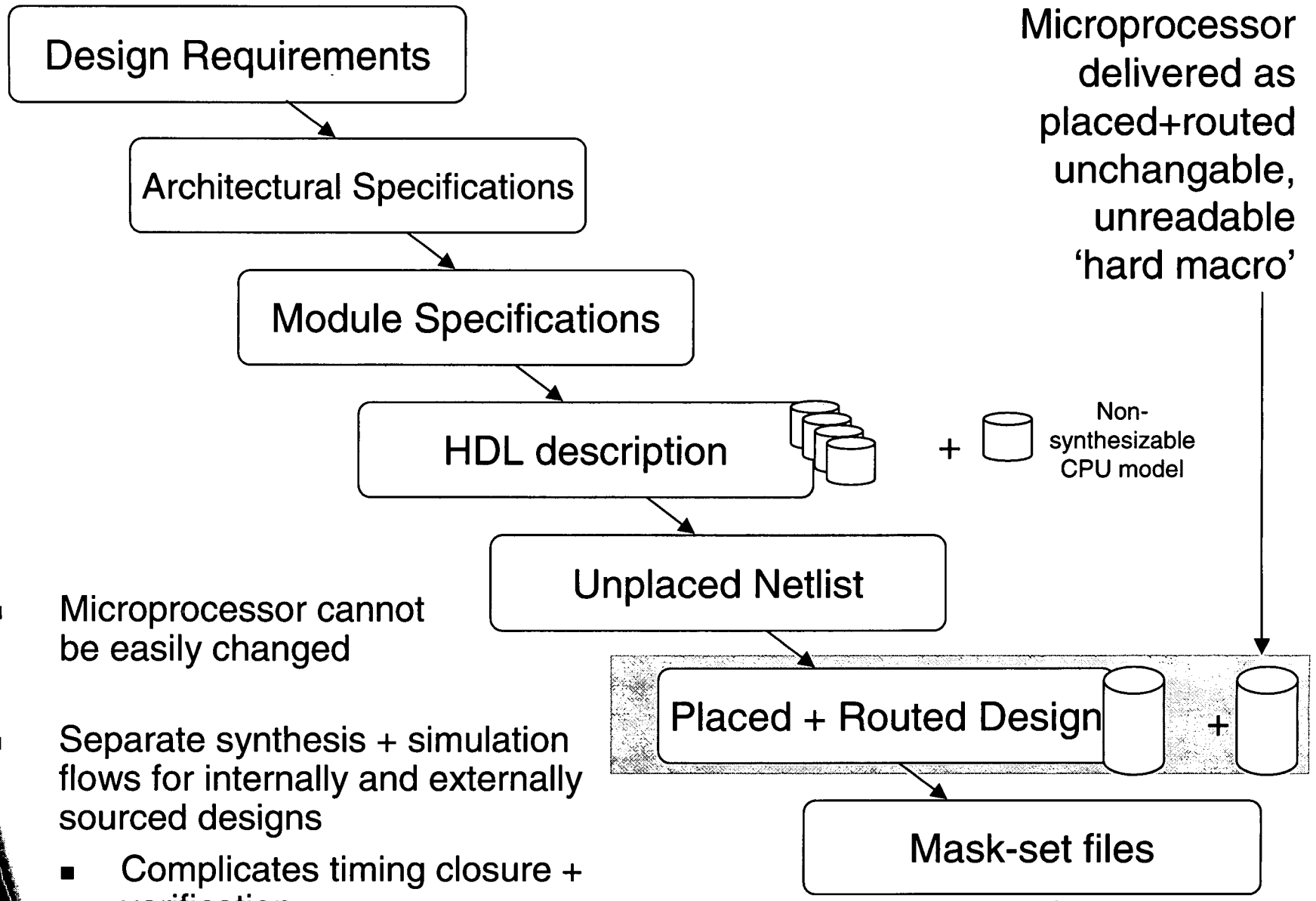
Translation steps



Syst m On Chip d sign

- Complete system on-chip created from
  - Internally sourced designs
    - Newly created designs
    - Pre-existing designs, modified for new application
  - Externally-sourced high-value Intellectual Property
    - Microprocessors
    - Complex Interface functions e.g. high-speed USB
  - Externally-sourced library functions
    - Standard cell logic libraries
    - Interface cell libraries
    - On-chip memory cells (e.g. RAMs)

In th tim b for our inv ntion...



- Microprocessor cannot be easily changed
- Separate synthesis + simulation flows for internally and externally sourced designs
  - Complicates timing closure + verification

ARC's inv ntion...

Design Requirements

Architectural Specifications

Module Specifications

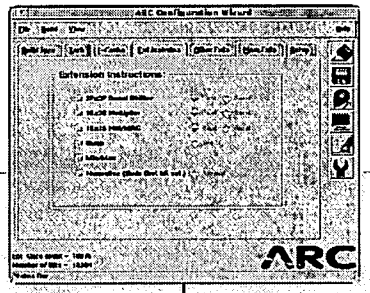
HDL description

Unplaced Netlist

Placed + Routed Design

Mask-set files

Microprocessor generated by tool as human-readable synthesizable HDL



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Microprocessor HDL can be easily recreated by selecting options in tool

Best CPU options can be determined to optimize a fixed design for the specific application

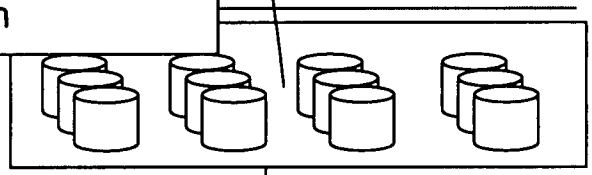
Application-specific extensions can be added by customer

Combined synthesis + simulation flows for internally and externally sourced designs

- Simplifies timing closure + verification

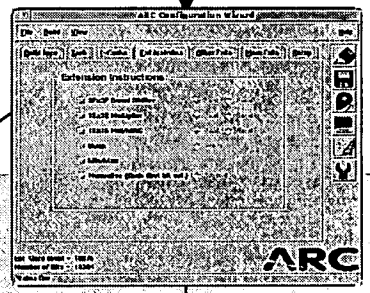
ARC's invention...

Library of basecase and extension CPU components specified in HDL, plus configuration and combination information



Design Requirements

Architectural Specifications



Module Specifications

HDL description + 

Unplaced Netlist

Placed + Routed Design

Mask-set files

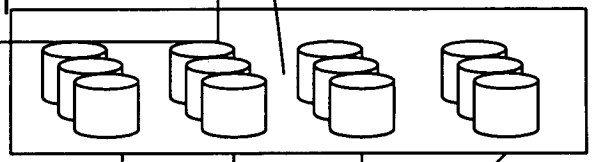
Tool can select CPU components at coarse level – e.g. presence of absence of instruction/data caches, ethernet or USB interfaces etc

Tool can configure CPU instruction set – e.g inclusion of special instructions like multiplier, CRC etc

Tool can perform fine-grain configuration, e.g. size + exact configuration of caches, number of interrupt signals, and combine components in most efficient way

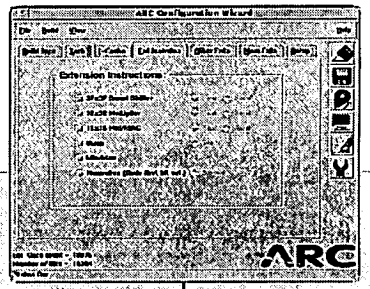
ARC's inv ntion...

Library of basecase and extension CPU components specified in HDL, plus configuration and combination information



Design Requirements

Architectural Specifications



Module Specifications

Tool can be used interactively, or controlled by a file which specifies the desired configuration

HDL description

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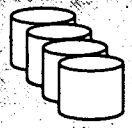
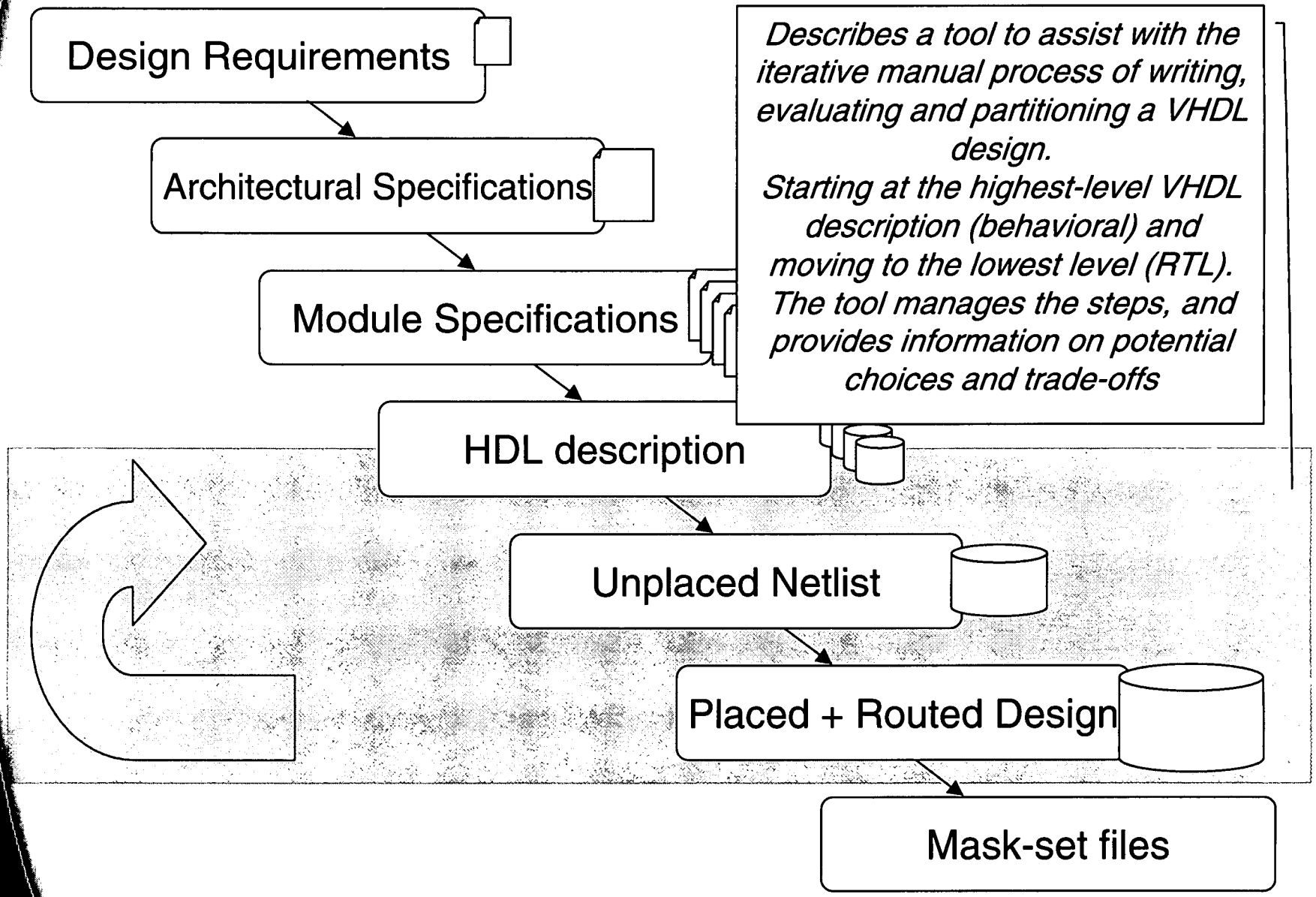


Unplaced Netlist

Placed + Routed Design

Mask-set files

Dangelo '678



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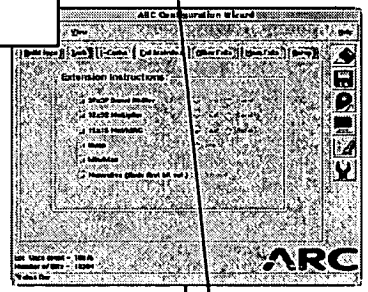
Produces functional description of customized microprocessor in the form of behavioral, RTL and structural VHDL files

Design Requirements

Architectural Specifications

Module Specifications



HDL description +

Dangelo

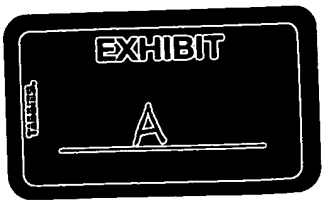
Unplaced Netlist

Placed + Routed Design

Operates using input HDL..
.. As produced by designers, and/or HDL generated by ARC tool

Ultimate result is a fixed-function device incorporating a programmable CPU

Mask-set files

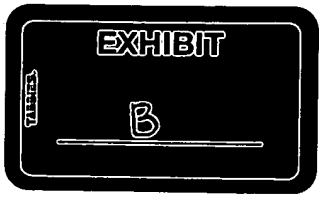


ARC International Royalty Summary

	Q2 '03	Q3 '03	Q4 '03	Q1 '04
Total Royalty Revenue	453,141	712,311	1,123,479	1,406,896
Total Chip Volume	2,479,022	2,455,449	8,146,159	14,743,237
Average Roy/Chip	0.18	0.29	0.14	0.10

210%

495%



ARC International Summary of Licensees

By Customer (in $ US)	Product Line		Code or Product
AM Logic	Processor	A4	
Brightcom/Flextronics	Processor	A4	
Catena	Processor	A3,A5	CNXA001AB
Cirrus Logic	Processor	A3	CS922XX Family
Cirrus Logic	Processor	A3	CS922XX Family
Cirrus Logic	Processor	A3	CS921XX Family
Corrent Corp.	Processor	V8	CR7120
Corrent Corp.	Processor	V8	CR7121
DS2	Processor	A3	DSS4200
DS2	Processor	A3	DSS4200
DS2	Processor	A3	DSS5100
DS2	Processor	A3	DSS5100
Fujitsu	Processor	A4, A5	MB86392PBS-G-NS3
Fujitsu	Processor	A4, A5	MB86392PBS-G-NS3-PIX
Fujitsu	Processor	A4, A5	MB86392PBS-G
Fujitsu	Processor	A4, A5	MB86392PBS-ES
Fujitsu	Processor	A4, A5	MB86392PBS-ES-NS2
Fujitsu	Processor	A4, A5	MB86392PBS-ES-NS3
Fujitsu	Processor	A4, A5	MB86394PFVS-G-BND
Fujitsu	Processor	A4, A5	MB86394PFVS-ES-BND
Fujitsu	Processor	A4, A5	MB86H20PMT-ES-BND
Fujitsu	Processor	A4, A5	MB86H21PMT-ES-BND
Fujitsu	Processor	A4, A5	MB86H21PMT-G-BND
Fujitsu	Processor	A4, A5	MB86H22PMT-ES-BND
Fujitsu	Processor	A4, A5	MB86H22PMT-G-BND
Fujitsu	Processor	A4, A5	MB87M214PMT-G-BND
Fujitsu	Processor	A4, A5	MB87K3081
Fujitsu	Processor	A4, A5	MB87K3081RB-ES
Fujitsu	Processor	A4, A5	MB87L2250
Fujitsu	Processor	A4, A5	MB87L2250-PFV-G-BND
Fujitsu	Processor	A4, A5	MB87M2141
Fujitsu	Processor	A4, A5	MB87M2141PMT-G-BND
Fujitsu	Processor	A4, A5	MB87M2142
Fujitsu	Processor	A4, A5	MB87M2142PMT-ES-BNI
Fujitsu	Processor	A4, A5	MB87M2142PMT-G-BND
Fujitsu	Processor	A4, A5	MB87M2143PMT-ES-BNI
Fujitsu	Processor	A4, A5	MB87M2143PMT-G-BND
Infineon	Processor	A3	A3
I***I	Processor	A3	Calexico

I***I	Processor	A3	Calexico
I***I	Processor	A3	Calexico
I***I	Processor	A3	IXF3208
I***I	Processor	A3	Calexico 2
I***I	Processor		
Leapfrog	Processor	A5	
Mansella	Processor	A4	ML1000
Qlogic	Processor	A4	multi
Sandisk	Processor	A5	20-99-00042-3
Sandisk	Processor	A5	20-99-00042-5
Sandisk	Processor	A5	20-99-00042-7
Sandisk	Processor	A5	20-99-00043-5
Sandisk	Processor	A5	20-99-00053-5
Sandisk	Processor	A5	20-99-00053-7
Sandisk	Processor	A5	20-99-00054-4
Sandisk	Processor	A5	20-99-00054-5
Sandisk	Processor	A5	20-99-00056-3
Sandisk	Processor	A5	20-99-00057-2
Sandisk	Processor	A5	20-99-00058-5
Top Layer Networks	Processor	A4	2500/3500
Vitesse	Processor	A3	VSC9186 Family
Vitesse	Processor	A3	VSC9188 Family

EXHIBIT

ARChitect™ Processor Configuration Tool

Introduction

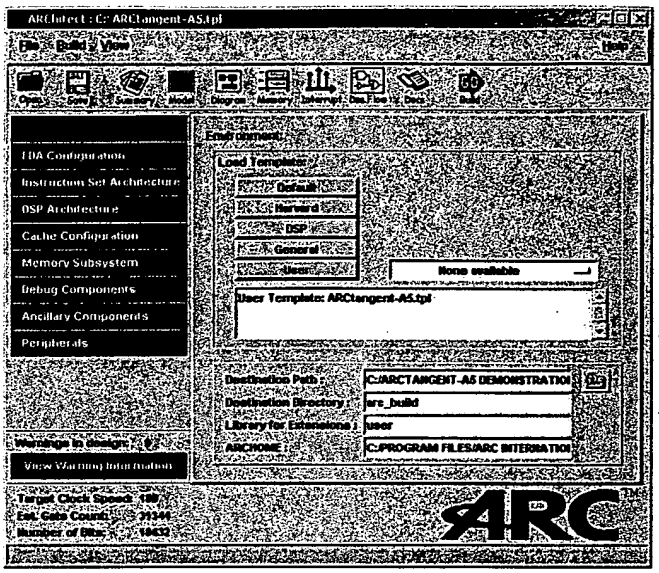
The ARChitect™ configuration tool allows developers to quickly and easily customize and extend the ARCtangent™ microprocessor core. It also lets developers integrate peripherals and other silicon intellectual property (IP). This ability to easily and quickly tailor the system to match the application means that developers do not have to waste valuable time integrating and verifying the processor and peripheral solution.

All a developer has to do is point and click through the configuration screens in the ARChitect tool, selecting the desired options. Summary screens and a system block diagram allow developers to easily visualize the configuration and check that every option chosen is correct. The ARChitect tool also provides guidelines for the size and memory requirements of the final processor design. Online help is available for each option, so developers can identify the best choices as they work their way through the configuration screens.

Developers can save their designs as templates for future modification. When a design is complete, clicking the Build button produces the source code (Verilog® or VHDL), synthesis scripts, test files, HDL-simulator support files, and HTML-formatted documentation for the design.

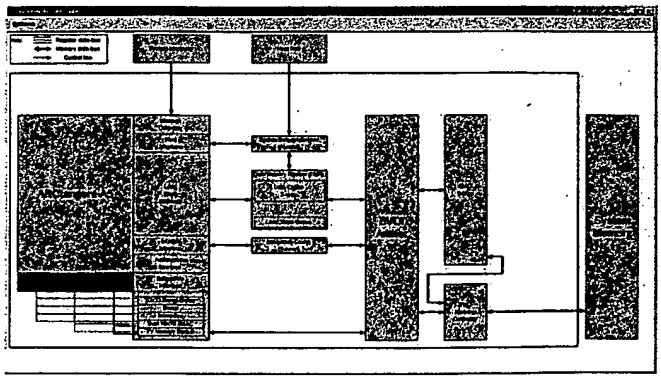
Feature List

- Simple processor configuration and extension with an easy-to-use graphical interface
- Design templates allow developers to create and recall standard designs for future modification
- System-architecture diagram provides a clear view of all components in the system and shows how they interconnect
- Updated information screens provide the designer with additional information, including estimated gate counts for each block, the selected instruction set, register configurations, and RAM allocation figures



The ARChitect configuration tool allows easy modification of the ARCtangent microprocessor

- Generates pre-verified, integrated Verilog/VHDL RTL source code, test benches, and HTML documentation
- Configuration options:
  - Microprocessor instruction set
  - DSP instructions/extensions
  - Instruction cache and data cache
  - Debug components
  - Interrupts
  - Pre-verified peripherals:
    - USB 1.1 Host/Device controller
    - USB 1.1 On-The-Go controller (ARCtangent-A5 only)
    - USB 2.0 Host/Device, On-The-Go (ARCtangent-A5 only)
    - UARTs
    - 10/100 Ethernet MAC
    - Timers



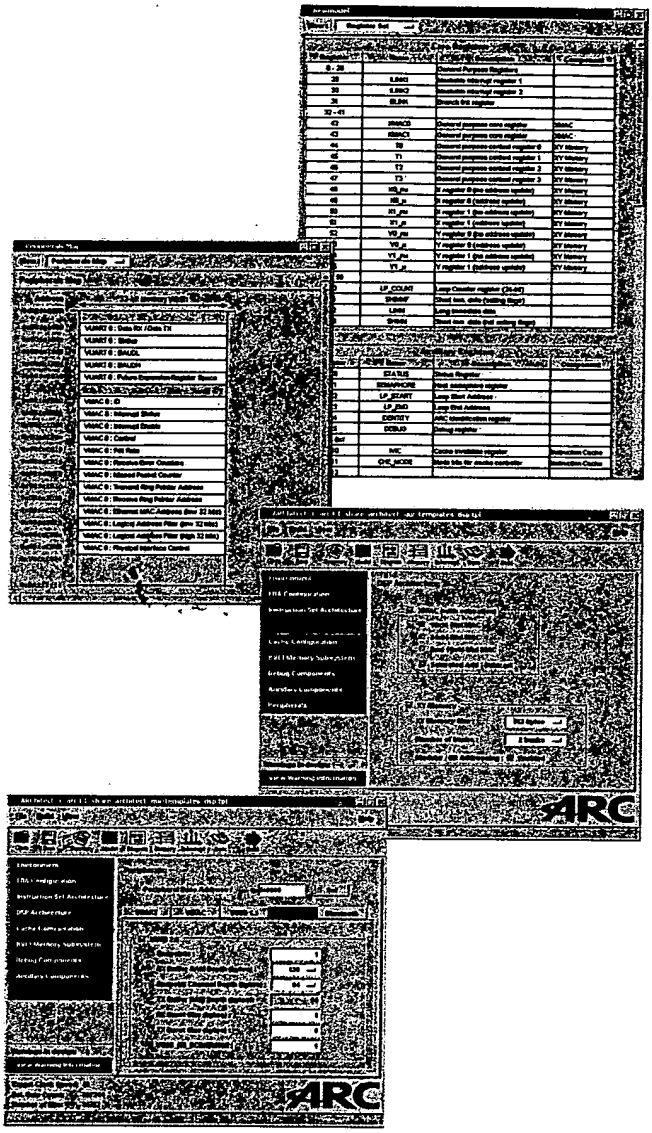
View the system block diagram to verify your design choices

Functional Description

The ARChitect configuration tool is a fast and powerful way for developers to customize the 32-bit ARCtangent microprocessor for specific applications. The graphical user interface has several intuitively grouped pages, making it easy for developers to quickly modify the processor design. Each design can be saved as a template for later recall and modification.

Additional information screens allow developers to effectively visualize the processor design. For example, the Programmer's Model screen provides software and firmware engineers with a complete list of all the instructions and registers that are part of the design. The System Architecture screen provides hardware engineers with a block diagram of the design.

The ARChitect tool builds all of the HDL files (Verilog or VHDL) in a directory of the developer's choice. It also generates other files required for synthesizing an ARCtangent processor, including the build descriptions, HTML documentation, test files, synthesis scripts, and simulator make-files.



System Requirements

- Sun™ Solaris™ or Microsoft® Windows 2000™
- Synopsys® Physical Compiler* (ARCtangent-A5 only)
- Synopsys® Design Compiler
- Synopsys DesignWare®
- HDL simulator:
  - Model Technology ModelSim®
  - Cadence NC-Verilog®
  - Cadence NC-VHDL
  - Synopsys VCS™

** optional*

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